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10/711,738	10/01/2004	Jen-Ying Chen	FTCP0043USA	5737

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EXAMINER	
DILLON, SAMUEL A	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
07/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/711,738	CHEN, JEN-YING	
	Examiner	Art Unit	
	SAMUEL DILLON	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Examiner acknowledges the applicant's submission of the amendment dated April 7, 2008. Per the amendment, Claims 1, 2, 8-10, 12 and 13 have been amended.

I. RESPONSE TO AMENDMENT(S) / ARGUMENT(S)

2. Applicant's arguments with respect to the 35 U.S.C. 103(a) rejections of Claims 1-10, 12 and 13 have been fully considered but they are **not persuasive**. The rejections have been upheld, and the Applicant directed below for traversal.

3. **The Applicant contends *(page 12)* that Riou does not teach counting how many data the configurable write buffer has ever stored and generating a write select value, and also does not teach counting how many data has ever been transferred to the single port memory and generating a read select value.**

The Examiner respectfully disagrees. Cucchi as combined with Riou would have two circular buffer counters as the read and write counters. As each counter would start at the initial location, whenever the number of writes or reads is less than the size of the buffer, the offset stored in the counter is proportional to the number of writes ever received or reads ever served respectively. Accordingly, Cucchi as combined with Riou does disclose counting how many data the configurable write buffer has ever stored and generating a write select value, and also counting how many data has ever been transferred to the single port memory and generating a read select value.

4. Regarding all other Claims not specifically traversed above and whose rejections were upheld, the Applicant contends that the listed claims are allowable by virtue of their dependence on other allowable claims. As this dependence is the sole rationale put forth for the allowability of said dependent claims, the Applicant is directed to the Examiner's remarks above.

Additionally, any other arguments the Applicant made that were not specifically addressed in this Office Action appeared to directly rely on an argument presented elsewhere in the Applicant's response that was traversed, rendered moot or found persuasive above.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 103 – Cucchi and Riou

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 1-10, 12 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cucchi et al. *(US Patent 4,899,352)* in view of Riou *(US Patent 5,649,146)*.

7. As per **Claim 1**, Cucchi disclose(s) a synchronous memory device with a single port memory unit, the synchronous memory device comprising:

the single port memory unit *(RAM 10, figure 3)* storing data according to a predetermined clock;

a configurable write buffer *(FIFO, figure 3)* electrically connected to the single port memory unit storing data according to the predetermined clock and transferring its stored data to the single port memory unit according to the predetermined clock *(FIFO is a dependency of the RAM access control logic, which is a dependency of ck channel, figure 3)*;

an arbiter *(RAM access control logic 18, figure 3)* electrically connected to the configurable write buffer and the single port memory unit generating the write acknowledge signal.

For the purposes of this rejection, Cucchi does not disclose the further limitations required by Claim 1. Riou discloses

a write blocking logic *(control circuitry, column 4 lines 4-33)* electrically connected to a configurable write buffer *(buffer, column 4 lines 4-33)* estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data according to the predetermined clock *(column 4 lines 4-33)*, and controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal *(implied is some way to signal the buffer to store a new value)*, wherein the write blocking logic comprises:

a first counter *(figures 1-2 show more than 4 buffer locations, meaning the register that stores the size must be more than 3 bits, in which case the first counter is interpreted as the first part of the register, column 2 lines 7-17)* counting the remaining data storage capability of the configurable write buffer;

a write select counter *(the output of the write address calculation, column 4 lines 4-33)* electrically connected to the first counter counting how many data the configurable write buffer has ever stored and generating a write select value *(the output of that counter)*; and

a read select counter *(the output of the read address calculation, column 4 lines 4-33)* electrically connected to the first counter counting how many data the configurable write buffer has ever transferred to the single port memory unit and generating a read select value *(the output of that counter)*; and the configurable write buffer comprises:

a plurality of buffer modules storing data *(figures 1-2)*;

a demultiplexer electrically connected to the buffer modules *(as the buffers are selected by an address and data is then stored to one of the plurality of places, this can*

be considered a demultiplexer, figures 1-2) storing data to the configurable write buffer according to the write select value; and

a multiplexer electrically connected to the buffer modules *(as the buffers are selected by an address and data is then retrieved from one of the plurality of places, this can be considered a multiplexer, figures 1-2)* transferring data stored in one of the buffer modules to the single port memory unit according to the read select value.

Cucchi and Riou are analogous art in that they both deal with write buffers. At the time of the invention it would have been obvious to a person having ordinary skill in the art to modify Cucchi to utilize Riou's modulo addressing buffer in place of the FIFO buffer. The motivation for doing so would have been that Riou's buffer provides a simple, fast buffer that can be of any size and has a short critical path to ensure fastest possible operation *(column 4 lines 4-14)*. Therefore, it would have been obvious to modify Cucchi's elastic buffer to replace the FIFO with Riou's circular buffer for the benefit of fast operation, to obtain the invention of Claim 1.

8. As per **Claims 2 and 12**, but more specifically to Claim 2, Cucchi and Riou disclose(s) the synchronous memory device of Claim 1, wherein the write blocking logic further comprises:

a write comparator *(Riou, column 4 lines 18-23)* electrically connected to the first counter comparing the remaining data storage capacity of the configurable write buffer counted by the first counter with a first predetermined count value and controlling the configurable write buffer to store data *(Riou, column 1 lines 56-67)*; and

a read comparator *(Riou, column 4 lines 18-23)* electrically connected to the first counter comparing the remaining data storage capacity of the configurable write buffer counted by the first counter with a second predetermined count value and controlling the configurable write buffer to transfer its stored data to the single port memory unit *(Riou, column 1 lines 56-67)*.

9. As per **Claim 3**, Cucchi and Riou disclose(s) the synchronous memory device of Claim 2, wherein the first counter has an initial count value equal to how many data the configurable write buffer can store and downward counts the remaining data storage capacity of the configurable write buffer *(Riou, column 4 lines 18-23)*, and the first predetermined count value is equal to zero *(the comparison is implied with be with a range of possible values, in which case the case of comparing with a logic zero in one of the bits is precluded)*.

10. As per **Claim 4**, Cucchi and Riou disclose(s) the synchronous memory device of Claim 3, wherein the write comparator controls the configurable write buffer to stop storing data when comparing that the remaining data storage capacity of the configurable write buffer is equal to zero *(Riou, implied by column 1 lines 15-30)*.

11. As per **Claim 5**, Cucchi and Riou disclose(s) the synchronous memory device of Claim 3, wherein the read comparator controls the configurable write buffer to stop transferring its stored data to the single port memory unit when comparing that the remaining data storage capacity of the configurable write buffer is equal to how many data the configurable write buffer can store *(Riou, implied by column 1 lines 15-30)*.

12. As per **Claim 6**, Cucchi and Riou disclose(s) the synchronous memory device of Claim 2, wherein the write select counter downward counts how many data the configurable write buffer has ever stored and generates the write select value *(Riou, column 4 lines 15-32)*.

13. As per **Claim 7**, Cucchi and Riou disclose(s) the synchronous memory device of Claim 2, wherein the read select counter downward counts how many data the configurable write buffer has ever transferred to the single port memory unit and generates the read select value *(Riou, column 4 lines 15-32)*.

14. As per **Claim 8**, Cucchi and Riou disclose(s) a synchronous\asynchronous memory device with a single port memory unit, the synchronous\asynchronous memory device comprising:

the single port memory unit *(Cucchi, RAM 10, figure 3)* storing data according to a read clock;

a configurable write buffer *(Riou's replacement of Cucchi's FIFO)* electrically connected to the single port memory unit storing data according to a write clock and transferring its stored data to the single port memory unit according to the read clock *(FIFO was a dependency of the RAM access control logic, which is a dependency of ck channel, figure 3)*;

a write blocking logic *(Riou, control circuitry, column 4 lines 4-33)* electrically connected to the configurable write buffer *(Riou, buffer, column 4 lines 4-33)* estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data according to the write clock *(Riou, column 4 lines 4-33)*, and controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal *(implied is some way to signal the buffer to store a new value)*, wherein the write blocking logic comprises:

a write counter *(Riou, register that stores highest location, figure 1)* counting the remaining data storage capability of the configurable write buffer;

a read counter *(Riou, register that stores lowest location, figure 1)* counting how many data in the configurable write buffer are ready to be transferred to the single port memory unit;

a write select counter *(Riou, the output of the write address calculation, column 4 lines 4-33)* electrically connected to the write counter counting how many data the

configurable write buffer has ever stored and generating a write select value *(Riou, the output of that counter)*; and

a read select counter *(Riou, the output of the read address calculation, column 4 lines 4-33)* electrically connected to the read counter counting how many data the configurable write buffer has ever transferred to the single port memory unit and generating a read select value *(Riou, the output of that counter)*; and

the configurable write buffer comprises:

a plurality of buffer modules *(Riou, figures 1-2)* storing data;

a demultiplexer *(Riou, as the buffers are selected by an address and data is then stored to one of the plurality of places, this can be considered a demultiplexer, figures 1-2)* electrically connected to the buffer modules storing data to one of the buffer modules according to the write select value; and

a multiplexer *(Riou, as the buffers are selected by an address and data is then retrieved from one of the plurality of places, this can be considered a multiplexer, figures 1-2)* electrically is connected to the buffer modules transferring data stored in one of the buffer modules to the single port memory unit according to the read select value; and

an arbiter *(Cucchi, RAM access control logic 18, figure 3)* electrically connected to the write blocking logic and the single port memory unit generating the write acknowledge signal.

15. As per **Claims 9 and 13**, but more specifically to Claim 9, Cucchi and Riou disclose(s) the synchronous\asynchronous memory device of Claim 8, wherein the write blocking logic further comprises:

a read\write synchronizer *(Riou, figure 3)* electrically connected between the write counter and the read counter changing signals synchronizing with the read clock to signals synchronizing with the write clock;

a write/read synchronizer *(Riou, figure 3)* electrically connected between the write counter and the read counter changing signals synchronizing with the write clock to signals synchronizing with the read clock;

a write comparator *(Riou, column 4 lines 18-23)* electrically connected to the write counter comparing the remaining data storage capacity of the configurable write buffer counted by the write counter with a first predetermined count value and controlling the configurable write buffer to store data *(Riou, column 1 lines 56-67)*; and

a read comparator *(Riou, column 4 lines 18-23)* electrically connected to the read counter comparing how many data in the configurable write buffer are ready to be transferred to the single port memory unit with a second predetermined count value and controlling the configurable write buffer to transfer its stored data to the single port memory unit according to the read clock *(Riou, column 1 lines 56-67)*.

16. As per **Claim 10**, Cucchi and Riou disclose(s) a computer system comprising:

a first computer *(Cucchi, first machine, column 1 lines 8-12)* operating on a first clock;

a second computer *(Cucchi, first machine, column 1 lines 8-12)*operating on a second clock different from the first clock; and

a memory device *(Cucchi, figure 2)* comprising:

a single port memory unit *(Cucchi, RAM 10, figure 3)* storing data according to the first clock;

a configurable write buffer *(Riou's replacement of Cucchi's FIFO)* electrically connected to the single port memory unit storing data transferred from the first computer according to the first clock and transferring its stored data to the single port memory unit according to the second clock *(Cucchi, FIFO was a dependency of the RAM access control logic, which is a dependency of ck channel, figure 3)*;

a write blocking logic *(Riou, control circuitry, column 4 lines 4-33)* electrically connected to the configurable write buffer *(Riou, buffer, column 4 lines 4-33)* estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data transferred from the first computer according to the first clock *(Riou, column 4 lines 4-33)*, and controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal *(implied is some way to signal the buffer to store a new value)*, wherein the write blocking logic comprises:

a write counter *(Riou, register that stores highest location, figure 1)* counting the remaining data store capability of the configurable write buffer;

a read counter *(Riou, register that stores lowest location, figure 1)* counting how many data in the configurable write buffer are ready to be transferred to the single port memory unit;

a write select counter *(Riou, the output of the write address calculation, column 4 lines 4-33)* electrically connected to the write counter counting how many data the configurable write buffer has ever stored and generating a write select value *(Riou, the output of that counter)*; and

a read select counter *(Riou, the output of the read address calculation, column 4 lines 4-33)* electrically connected to the read counter counting how many data the

configurable write buffer has ever transferred to the single port memory unit and generating a read select value *(Riou, the output of that counter)*; and

the configurable write buffer comprises:

a plurality of buffer modules *(Riou, figures 1-2)* storing data;

a demultiplexer *(Riou, as the buffers are selected by an address and data is then stored to one of the plurality of places, this can be considered a demultiplexer, figures 1-2)* electrically connected to the buffer modules storing data to one of the buffer modules according to the write select counter value; and

a multiplexer *(Riou, as the buffers are selected by an address and data is then retrieved from one of the plurality of places, this can be considered a multiplexer, figures 1-2)* electrically is connected to the buffer modules transferring data stored in one of the buffer modules to the single port memory unit according to the read select value: and

an arbiter *(Cucchi, RAM access control logic 18, figure 3)* electrically connected to the write blocking logic and the single port memory unit generating the write acknowledge signal.

III. CLOSING COMMENTS

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

a. **STATUS OF CLAIMS IN THE APPLICATION**

18. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). CLAIMS NO LONGER IN THE APPLICATION

19. Claim 11 was cancelled by amendment.

a(2). CLAIMS REJECTED IN THE APPLICATION

20. Per the instant office action, Claims 1-10, 12 and 13 have received an action on the merits and are subject of a final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 9:30-6:00.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sam Dillon
Examiner
Art Unit 2185

SAD

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Primary Examiner, Art Unit 2185